cont. 2
a1

a metal insulator semiconductor transistor formed in said semiconductor substrate, having a source or drain region of [the other] another conduction type which is connected to said second conductive layer, said first conductive layer being isolated from said source or drain region.

Claim 2, line 3, delete "other" and insert therefor --another--;

---

c. 3

3. (Once Amended) A memory according to claim 1, wherein [a predetermined interval is formed between the] an upper end portion of said first conductive layer and [the] a bottom level of said source or drain layer are separated by a predetermined distance.

Claim 4, line 2, delete "interval" and insert therefor --distance--;

Claim 5, line 2, before "adjacent" delete "in";

REMARKS

This amendment responds to the Office Action dated December 1, 1987, in which the Examiner rejected claims 3 and 4 under 35 U.S.C. 112, rejected claims 1, 2, 5, 6 and 8 under 35 U.S.C. 102(1) and/or (b) and under 35 U.S.C. 103, and rejected claims 3, 4 and 7 under 35 U.S.C. 103.

As indicated above, minor informalities in the specification have been corrected. It is respectfully requested that the Examiner approve the corrections.

Claims 3 and 4 were rejected under 35 U.S.C. 112. As indicated above, the claims have been amended in order to more particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is respectfully submitted that the rejection of the claims under 35 U.S.C. 112 no longer applies. Therefore, it is respectfully requested that the Examiner withdraw the rejection to the claims under 35 U.S.C. 112.

Claim 1 has been amended to claim a random access memory having a trench capacitor. The memory comprises a semiconductor substrate, a trench, first and second conductive layers, a dielectric layer and a metal insulator semiconductor transistor. The semiconductor substrate is of one conductivity type. The trench is formed in the semiconductor substrate. The first conductive layer is formed on a deep portion of an inner surface of the trench and is not formed in a region close to an entrance of the trench. The dielectric layer is formed on the first conductive layer in the trench and is formed on the inner surface of the trench in the region close to the entrance of the trench. The second conductive layer fills in the trench through the dielectric layer. The first conductive layer, the dielectric layer and the second conductive layer constitute a storage capacitor. The metal insulator semiconductor transistor is formed in the semiconductor substrate. The metal insulator semiconductor transistor has a source or drain region of another conductivity type which is connected to the second conductive layer. The first conductive layer is isolated from the source or drain region.

Through the structure of the present invention having a first conductive layer formed in a deep portion of an inner surface of the trench and not being formed in a region close to the entrance of the trench and having a dielectric layer formed on the first conductive layer in the trench and formed on the inner surface of the trench in the region close to the entrance of the trench, as claimed in amended claim 1, the present invention provides a dynamic random access memory in which the punch-through phenomena between adjacent trench capacitors is prevented. In addition, through the structure of the present invention, the possibility of soft errors is reduced. The prior art does not show, teach or suggest a first conductive layer formed in only a deep portion of an inner surface of a trench and not formed in a region close to the entrance of the trench and having a dielectric layer which is formed on the first conductive layer and is formed on the inner surface of the trench in the region close to the entrance of the trench as claimed in amended claim 1.

Claims 1, 2, 5, 6 and 8 were rejected under 35 U.S.C. 102(a) and/or (b) as being anticipated by, or in the alternative under 35 U.S.C. 103, as being obvious over Sunami et al (European Application No. 0108390).

Sunami et al appears to disclose a bit line 3, word lines 4-1 and 4-3, a plate 8, a substrate 10, a first intermediate insulating film 13, a second intermediate insulating film 14, diffusion layer 15, grooves 17, capacitor insulating film 18 and capacitor electrode 19. The capacitor 1 is made up of the capacitor insulating film 18 and two

electrodes, a) the capacitor electrode 19 and b) the plate 8 on either side of the capacitor insulating film 18.

Thus, Sunami et al merely discloses a plate 8, a capacitor insulating film 18 and a capacitor electrode 19. Sunami et al does not show, teach or suggest a first conductive layer formed on a deep portion of an inner surface of a trench and not being formed in a region close to an entrance of a trench as claimed in amended claim 1. Rather, Sunami et al teaches away from the present invention since in Sunami et al the plate 8 is formed in the region close to the entrance of the trench.

A second distinction between the present invention and Sunami et al is that Sunami et al does not show, teach or suggest a dielectric layer formed on the first conductive layer in the trench and formed on the inner surface of the trench in the region close to the entrance of the trench as claimed in amended claim 1. The insulating film 18 of Sunami et al is not formed on the inner surface of the trench in the region close to the entrance of the trench. Rather, the insulating film 18 is only formed on the first conductive layer and is never formed on the inner surface of the trench. The insulating film 18 is formed on the top surface of the substrate over the entrance of the trench on top of the plate 8. This is completely different from the present invention in which the dielectric layer is formed on the inner surface of the trench at the entrance of the trench as claimed in amended claim 1.

Since Sunami et al does not show, teach or suggest a) a first conductive layer formed on a deep portion of an inner surface of a trench and not formed in a region close to an entrance of the trench and b) a dielectric layer which is formed

on the first conductive layer in the trench and which is formed on the inner surface of the trench in the region close to the entrance of the trench, as claimed in amended claim 1, it is respectfully requested that the Examiner withdraw the rejection to claim 1 under 35 U.S.C. 102(a), 35 U.S.C. 102(b) and 35 U.S.C. 103.

Claim 2 depends from claim 1 and recites the additional feature that the second conductive layer is electrically connected with the source or drain region of another conductivity type through a third conductive layer.

Claim 5 depends from claim 1 and recites the additional feature that the source or the drain region is adjacent the second conductive layer through the dielectric layer.

Claim 6 depends from claim 1 and recites the additional feature that the first conductive layer is in contact with the semiconductor substrate in the trench.

Claim 8 depends from claim 1 and recites the additional feature that the dielectric layer has a larger thickness at the surface of the semiconductor substrate than on the first conductive layer.

It is respectfully submitted that the claims 2, 5, 6 and 8 are not anticipated by or are obvious within the meaning of 35 U.S.C. 102(a), 35 U.S.C. 102(c) and 35 U.S.C. 103 over Sunami et al for the reasons as set forth above with respect to amended claim 1. Therefore, it is respectfully requested that the Examiner withdraw the rejection to claims 2, 5, 6 and 8 under 35 U.S.C. 102(a), 35 U.S.C. 102(b) and under 35 U.S.C. 103.

Claims 3 and 4 were rejected under 35 U.S.C. 103 as being unpatentable over Sunami et al and further in view of Miura et al (U.S. Patent No.4,672,410).

Miura et al appears to disclose a semiconductor device having a substrate 11, bit line 12, word line 13, trench capacitor 14, isolation region 15, cell plate 16, isolation region 17, insulating films 18 and source/drain regions 19.

Miura et al does not show, teach or suggest a first conductive layer formed in a deep portion of the an inner surface of a trench and not formed in a region close to an entrance of the trench as claimed in amended claim 1. Furthermore, Miura et al does not show, teach or suggest a dielectric layer being formed in the first conductive layer in the trench and being formed on the inner surface of the trench in the region close to the entrance of the trench as claimed in amended claim 1. The trench capacitor 14, an isolation region 15 and a cell plate 16 of Miura et al merely discloses a cell plate formed inside the trench capacitor which is opposite the present invention. The combination of Miura et al with Sunami et al would suggest the structure of Sunami et al using a cell plate inside the trench capacitor as taught by Miura et al. Thus, the combination does not show, teach or suggest the invention as claimed in amended claim 1.

Claim 3 depends from claim 1 and recites the additional feature that an upper end portion of the first conductive layer and a bottom level of the source or drain layer are separated by a predetermined distance.

Claim 4 depends from claim 3 and recites the additional feature that the predetermined distance is occupied by an insulator material.

It is respectfully submitted that claims 3 and 4 are not obvious within the meaning of 35 U.S.C. 103 over Sunami et al and Miura et al for the reasons as set forth above with respect to amended claim 1. Therefore, it is respectfully requested that the Examiner withdraw the rejection to claims 3 and 4 under 35 U.S.C. 103.

Claim 7 was rejected under 35 U.S.C. 103 as being unpatentable over Sunami et al and further in view of Murao (Japanese Kokai 58-213640).

Murao appears to disclose a groove formed selectively in a substrate 100 and a phosphorous-doped polysilicon serves as the first capacitance electrode 103.

Thus, Mural does not show, teach or suggest a first conductive layer formed in a deep portion of an inner surface of a trench and not being formed in a region close to an entrance of the trench or a dielectric layer being formed on the first conductive layer in the trench and being formed on the inner surface of the trench in the region close to the entrance of the trench as claimed in amended claim 1. The combination of Sunami et al and Murao would merely suggest to use the structure of Sunami et al using a phosphorus-doped polysilicon as the first capacitance electrode. Thus, the combination does not show, teach or suggest the invention as claimed in amended claim 1.

Claim 7 depends from claim 1 and recites the additional feature that the first conductive layer comprises a polycrystalline silicon.

It is respectfully submitted that claim 7 is not obvious within the meaning of 35 U.S.C. 103 over Sunami et al and Miura et al for the reasons as set forth above with respect to amended claim 1. Therefore, it is respectfully requested that the Examiner withdraw the rejection to claim 7 under 35 U.S.C. 103.

Thus it now appears that the application is in condition for allowance. Reconsideration and allowance at an early are respectfully requested.

If for any reason the Examiner feels the application is not now in condition for allowance, it is respectfully requested that he contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2395, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, NIKAIDO, MARMELSTEIN & KUBOVCIK

By: _____

Ellen Marcie Emas
Attorney for Applicant
Registration No. 32,131

Attorney Docket No.
P21-698-AM87145

Suite 912,
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930
EME/ghb
Enclosures: Petition for 3-Month Extension of Time; Information Disclosure Statement.